What is claimed is:

1. A display apparatus drive circuit having a phase adjustment circuit in a driver for driving a display apparatus based on inputted clock and data, said phase adjustment circuit comprising:

a first synchronous delay circuit for adjusting a duty of said inputted clock and outputting it as a first clock,

a second synchronous delay circuit for delaying said adjusted clock by a predetermined delay amount and outputting it as a second clock,

a first holding circuit for holding and outputting said data in response to said first clock, and

a second holding circuit for holding and outputting the data outputted from said first holding circuit in response to said second clock.

2. The display apparatus drive circuit according to claim 1, wherein said phase adjustment circuit comprises a third holding circuit for holding and outputting a start pulse in response to said first clock and a fourth holding circuit for holding and outputting the start pulse outputted from said third holding circuit in response to an inversion signal of said first clock.

3. The display apparatus drive circuit according to claim 1, wherein said driver further comprises a data latch circuit for operating in response to the data outputted from said phase adjustment circuit and said first clock signal.

4. The display apparatus drive circuit according to claim 1, wherein said first synchronous delay circuit outputs said inputted clock by setting its duty ratio at 50 percent.

5. The display apparatus drive circuit according to claim 2, wherein said second synchronous delay circuit outputs said first clock by delaying it by $\pi/2$.

6. The display apparatus drive circuit according to claim 5, wherein said data latch circuit takes in data on a leading edge and a trailing edge of said first clock.

7. The display apparatus drive circuit according to claim 6, wherein said data latch circuit comprises a selector circuit for alternately outputting the data latched on said leading edge of said first clock and the data latched on said trailing edge thereof.

8. A display apparatus drive circuit having a plurality of drivers for driving a display apparatus based on inputted clock and data, each of said plurality of drivers comprising:

a first synchronous delay circuit for adjusting a duty ratio of the inputted clock and outputting it as a first clock,

a second synchronous delay circuit for delaying said first clock by a predetermined delay amount and outputting it as a first delay clock,

a first phase adjustment circuit for holding and outputting the data inputted based on said first clock and said first delay clock,

a latch circuit for holding said held and outputted data in response to said first clock,

a third synchronous delay circuit for readjusting the duty ratio of said first clock and supplying it as a second clock to a next-stage driver,

a fourth synchronous delay circuit for delaying said second clock by the predetermined delay amount and outputting a second delay clock, and

a second phase adjustment circuit for holding the data inputted based on said second clock and said second delay clock and outputting the held data to said next-stage driver.

9. The display apparatus drive circuit according to claim 8, further comprising a latch circuit for latching a start pulse in response to said first clock.

10. The display apparatus drive circuit according to claim 8, wherein it comprises a first latch circuit for latching and outputting the data inputted in response to said first clock and said first delay clock.

11. The display apparatus drive circuit according to claim 10, wherein it comprises a second latch circuit for latching and outputting the data inputted in response to said second clock and said second delay clock.